AN3261
Application note

Dual push-button Smart Reset™ devices with user-adjustable setup delays

Introduction

The Smart Reset™ family of devices consists of several products with a combination of features selected to best suit most typical applications. Their basic common feature is dual-button reset with setup delay that requires both input reset buttons to be continuously pressed for a defined period of time. This improves system stability compared to simple manual reset button devices and eliminates the need for a traditional reset access hole (e.g. two standard keys on the mobile phone keyboard can be used as Smart Reset™ inputs). Numerous additional features and device options are factory-programmed or can be implemented upon request.

Common STM65xx Smart Reset™ family features include:

- Dual-button Smart Reset™ inputs
- V_{CC} range 1.0 to 5.5 V (active-low output valid)
- Industrial operating temperature range –40 °C to +85 °C
- Space-saving TDFN8 package (2 mm x 2 mm x 0.75 mm)
- RoHS compliance

Differentiating features of the devices are:

- With or without Power-on Reset (POR)
- With or without V_{CC} monitoring
- Independent battery monitoring feature with battery-low warning (STM6505 only)
- Input logic voltage levels: standard CMOS or fixed threshold
- Smart Reset™ output characteristics
  - Defined reset pulse duration or push-button controlled (undefined) reset pulse duration
  - Reset pulse duration: factory-programmed or capacitor-adjustable
  - Smart Reset™ delay: tri-state / dual-state / capacitor-adjustable
  - Open-drain or push-pull reset output
  - Single or dual reset output

Contents

1 **Features** 4

2 **Typical application diagrams** 5

2.1 Single-button reset 5

2.2 Dual-button reset 7

2.3 Multiple-button reset 8

2.4 Input pull-up considerations (CMOS/fixed levels) 9

2.5 Output pull-up considerations 9

2.6 Reliability note 10

3 **Demonstration boards, promotion tools** 11

3.1 STM6503 demonstration board 11

3.2 STM65xx interposer boards 12

3.3 Smartphone demonstration example 13

4 **Conclusion** 15

5 **Revision history** 16

List of figures

Figure 1. Single-button Smart Reset™ typical application diagram, with “early-warning” feature, STM6503 5
Figure 2. Timing diagram - single push-button Smart Reset™ 6
Figure 3. Dual push-button Smart Reset™ typical application diagram, STM6503 7
Figure 4. Timing diagram - dual push-button Smart Reset™ 7
Figure 5. Three push-button delayed Smart Reset™ typical application diagram, STM6503 8
Figure 6. Timing diagram - three push-button Smart Reset™ 9
Figure 7. Smart Reset™ demonstration board, STM6503 11
Figure 8. The STM65xx interposer boards; a dedicated board is available for each STM65xx Smart Reset™ device 12
Figure 9. Smartphone demonstration example shows STM6503 implemented in an actual application 13
Figure 10. Smart Reset™ demonstration in an actual smartphone application 14

1 Features

- The **Smart Reset™** functionality is a feature that introduces a reset output response delay. Both of the Smart Reset™ input buttons must be pressed for a defined t_{SRC} period, only after which an output reset pulse is generated. This results in a robust hardware reset. The reset function can then be assigned to the existing keys of a device, which eliminates the traditional reset hole in the back cover of the device, while maintaining system stability. All the STM65xx family devices have this feature with the exception of the STM6504.
- The **edge trigger** functionality is a reset input with an immediate reset response and a special debounce feature. Found only on the STM6504 (a device with single-button edge trigger immediate reset and a single-button delayed Smart Reset™ input, independent but with a common reset output).
- **V_{CC} monitoring/undervoltage reset**. When the monitored V_{CC} voltage drops below the factory-programmed undervoltage reset threshold V_{RST}, the reset output(s) immediately go active and remain so until V_{CC} rises above V_{RST} and hysteresis, plus the defined t_{REC} period.
- **Battery-low detection** is an additional independent voltage monitoring function with a dedicated battery-low detection output pin. It works as a pure comparator with V_{REF}=1.25 V. STM6505 only.
- **Fixed input logic levels** are suitable for configurations where the device driving the input buttons (keyboard) is connected to a lower voltage than the supply voltage of the STM65xx device. This is in contrast to the devices with the standard CMOS input logic levels that are relative to V_{CC} and are suitable only for applications in which the device driving the inputs of the Smart Reset™ device is powered by the same voltage supply.

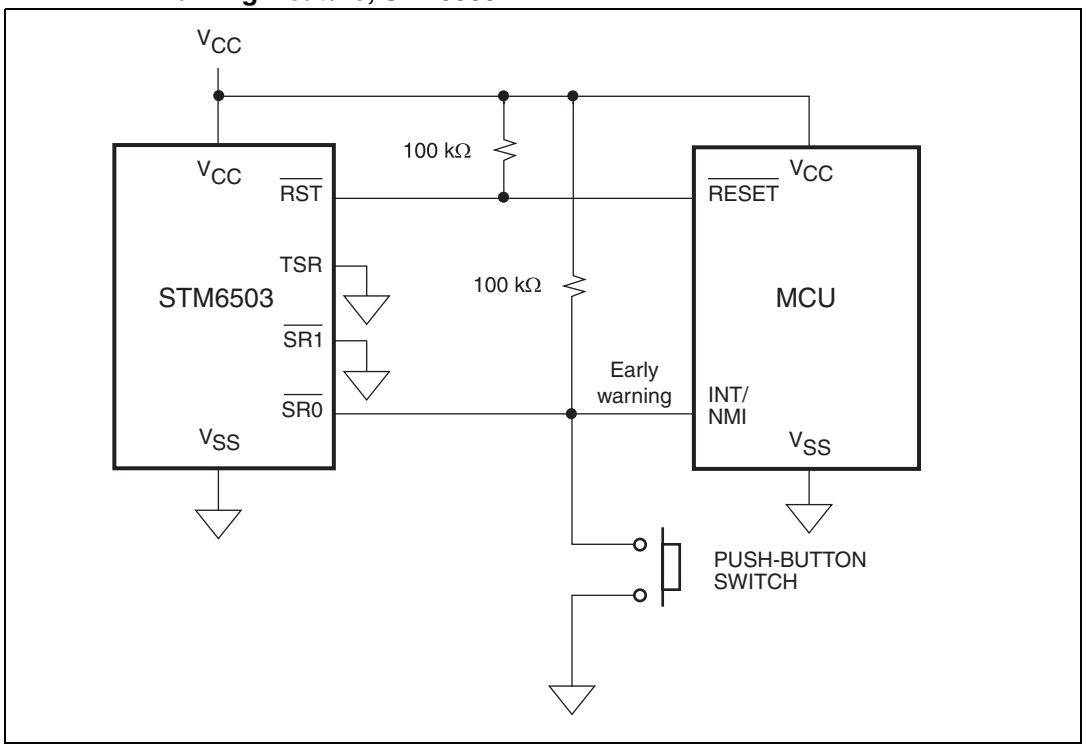
2 Typical application diagrams

The STM65xx family of Smart Reset™ products provides a broad variety of options for various types of applications.

2.1 Single-button reset

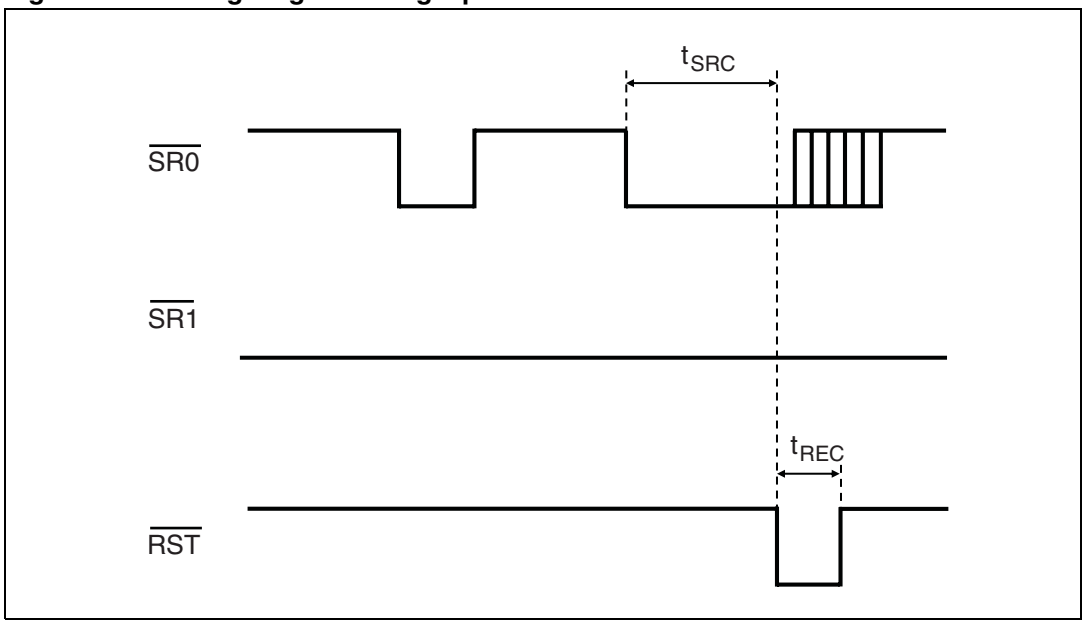
The STM65xx devices allow for different reset input configurations. In simple applications, only one input reset button with delayed reset may be sufficient. In this case, for product options without internal input pull-up resistors, $\overline{SR0}$ and $\overline{SR1}$ can be either connected together or the unused $\overline{SR}$ input permanently grounded. In the case of a product version with internal input pull-up resistors, just connect the inputs together. Permanent grounding of the unused $\overline{SR}$ input would, in this case, cause a continuous current to flow through the pull-up resistor from V_{CC} to V_{SS}.

Figure 1. Single-button Smart Reset™ typical application diagram, with "early-warning" feature, STM6503



1. Early warning feature: the input reset push-button can be also used as an early warning to the processor (through the interrupt input) that a reset may come after the t_{SRC} reset setup delay.

Figure 2. Timing diagram - single push-button Smart Reset™



2.2 Dual-button reset

The most frequent application requires a configuration with two reset buttons which further improves immunity to undesired resets by adding a second input reset button with delayed reset. In this case, the reset pulse occurs only when both the buttons have been pressed and held for the defined t_{SRC} delay.

Figure 3. Dual push-button Smart Reset™ typical application diagram, STM6503

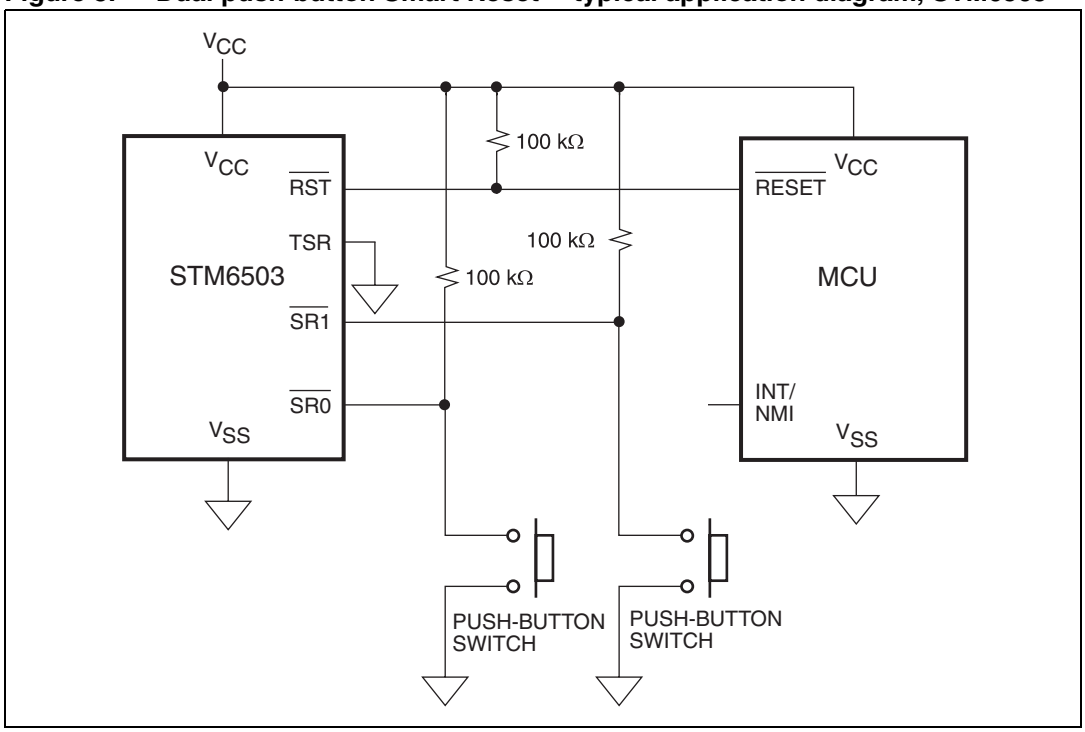
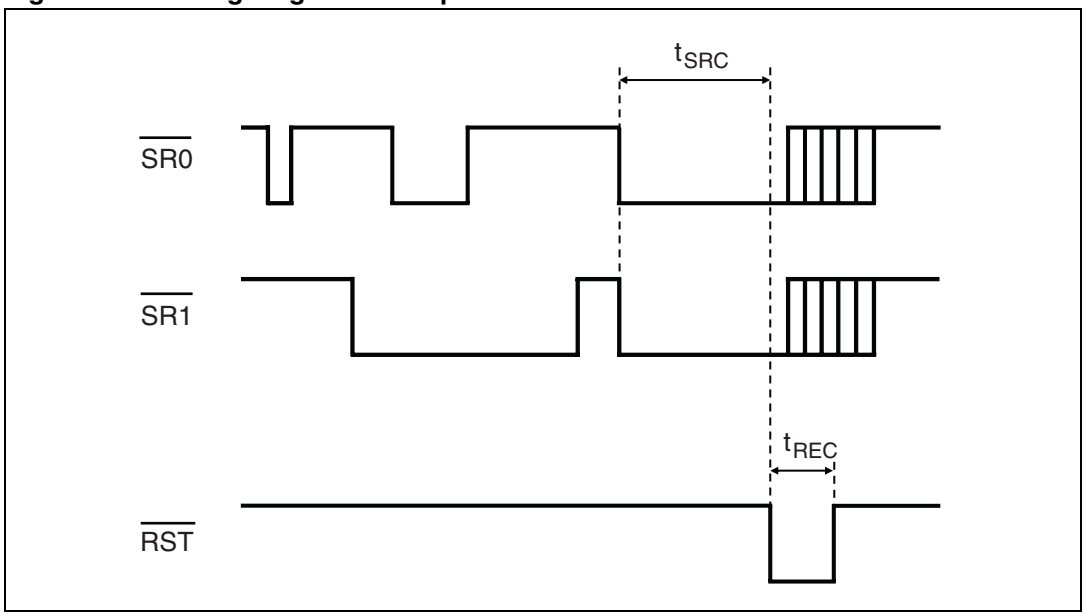


Figure 4. Timing diagram - dual push-button Smart Reset™



2.3 Multiple-button reset

Adding even more input buttons is possible by adding a simple OR gate. All of the buttons must then be pressed simultaneously for at least t_{SRC} input delay seconds to get a reset pulse on the STM65xx output. For a configuration with three input reset buttons, connect one button to one $\overline{SR}$ input as usual and the remaining two buttons to an OR gate and tie its output to the second $\overline{SR}$ input.

Figure 5. Three push-button delayed Smart Reset™ typical application diagram, STM6503

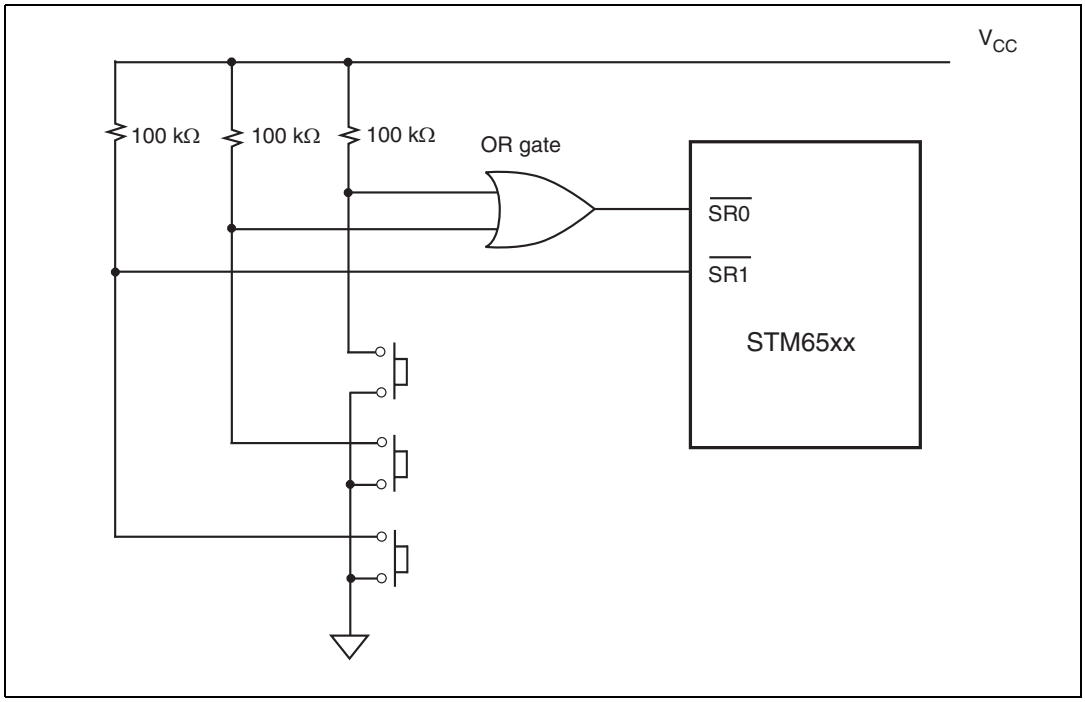
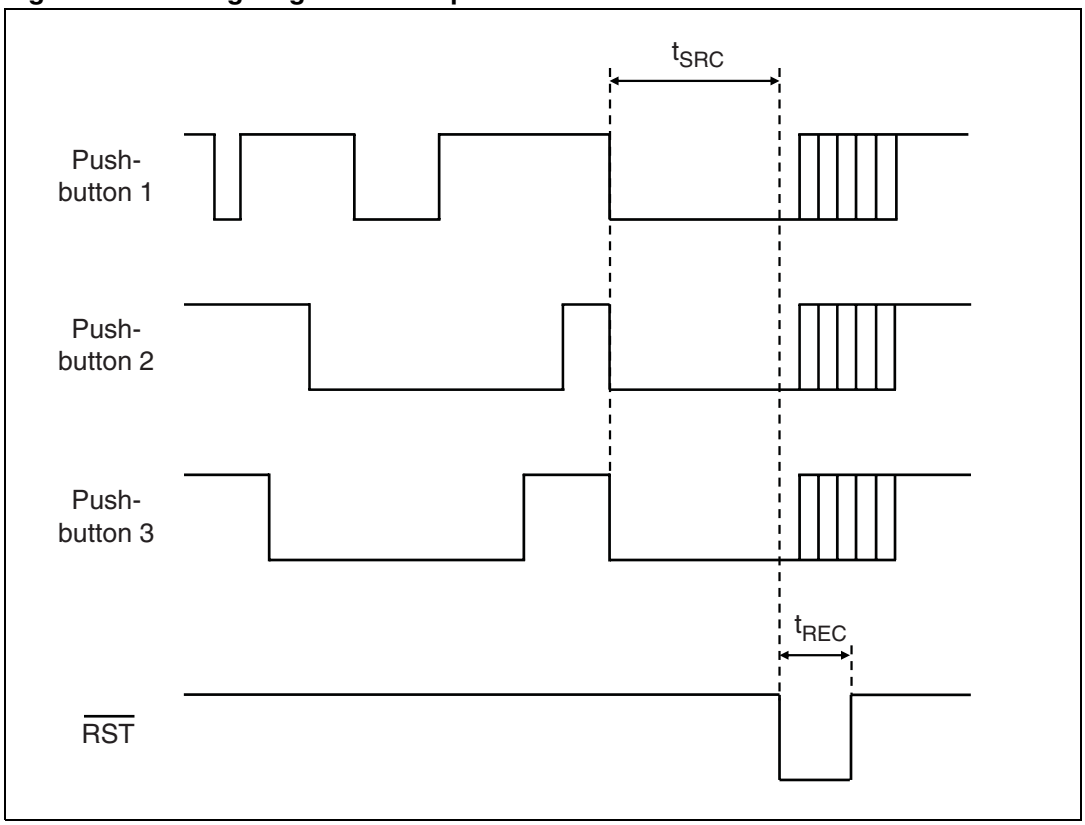


Figure 6. Timing diagram - three push-button Smart Reset™



2.4 Input pull-up considerations (CMOS/fixed levels)

Inputs without internal pull-up resistors can be pulled to a different voltage level than the supply voltage of the STM65xx devices, however:

- the input pull-up voltage level should not exceed 5.5 V
- the input logic levels specifications must be respected:
  - V_{IH}min = 0.7V_{CC}, V_{IL}max = 0.3V_{CC} in case of standard CMOS input cells (it is recommended to always keep V_{IL} on the ground level and V_{IH} on the V_{CC} level)
  - V_{IH}min = 0.85 V, V_{IL}max = 0.3 V in case of the fixed-logic levels devices (STM6520, STM6522).

2.5 Output pull-up considerations

Open-drain $\overline{RST}$ outputs without internal pull-up resistors can also be pulled up to any voltage independent of V_{CC} (higher or lower than V_{CC}) (but absolute maximum ratings must be respected). The STM65xx devices can thus serve also as a simple level shifter.

2.6 Reliability note

Devices with timings adjusted by external components vs. environmental considerations

For device options with timings (t_{SRC}, t_{REC}) adjusted by an external capacitor, there are several additional factors to be considered that may affect the accuracy of the timings. The given specifications apply to the STM65xx device alone, i.e. with an ideal timing capacitor. External tolerances, temperature dependencies and leakages are excluded.

The Smart Reset™ devices are designed to meet strict requirements for the lowest possible current consumption and to maintain the common timing constant 10 s/µF, therefore the constant current used to charge the external timing capacitor is very low, in the magnitude of 100 nA. Any external leakage (e.g. poor quality timing capacitors or excessive humidity, especially if dew-point is exceeded and moisture condensation occurs on the PCB tracks) may cause a significant leakage current which is deducted from the constant charging current that the device provides, reducing the effective external timing capacitor charging current which results in extending the t_{SRC} (t_{REC}) timings. To minimize this effect, the PCB tracks between the SRC ($TREC_{ADJ}$) pin and its respective timing capacitor should be as short as possible, properly covered with solder mask and isolated from other tracks (especially V_{SS}) by as great a distance as possible. Also, low-leakage timing capacitors (ceramic or film capacitor) should be used.

3 Demonstration boards, promotion tools

A complete set of demonstration/promotion tools is available for various purposes, from easy, high-level application functional demonstration, down to tools for detailed testing. These tools are based on the STM6503 as the primary representative of the Smart Reset™ family, as the basic Smart Reset™ functionality is common.

3.1 STM6503 demonstration board

Purpose

The demonstration board serves as a functional demonstration of the Smart Reset™ devices and the easily accessible test points provide for basic measurements and testing.

Figure 7. Smart Reset™ demonstration board, STM6503

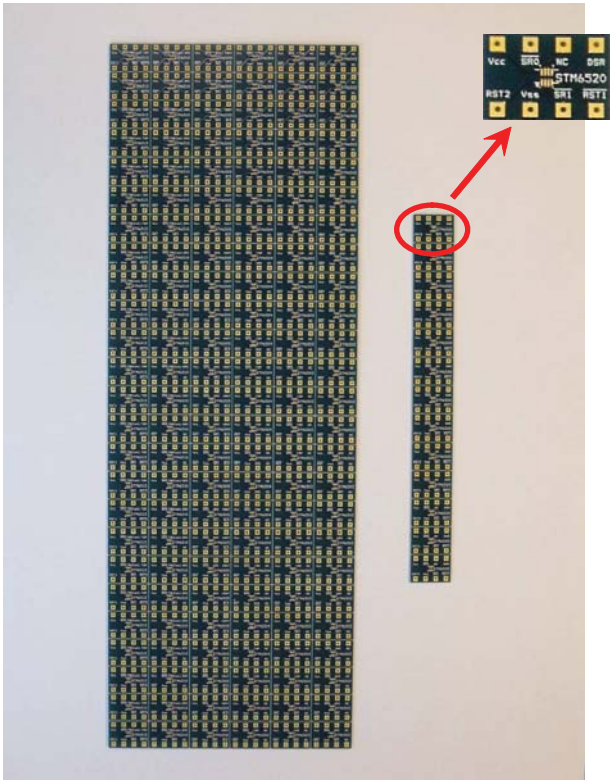
- Simultaneous push of the SR0 and SR1 buttons is indicated by an LED
- LED and audible indication of the reset pulse after t_{SRC} reset delay
- Test points available for easy tracking of the Smart Reset™ signals
- Jumper-selectable Smart Reset™ delay (2/6/10 seconds minimum)

3.2 STM65xx interposer boards

Purpose

The dedicated interposer PC boards were created for each STM65xx Smart Reset™ device for a quick and flexible application/testing setup preparation. The boards include labels on each pin for easy identification. The pitch of the interposer pins easily fits into a breadboard and allows a very flexible application setup testing, or soldering wires for external connections (to a tester for example).

Figure 8. The STM65xx interposer boards; a dedicated board is available for each STM65xx Smart Reset™ device



3.3 Smartphone demonstration example

Purpose

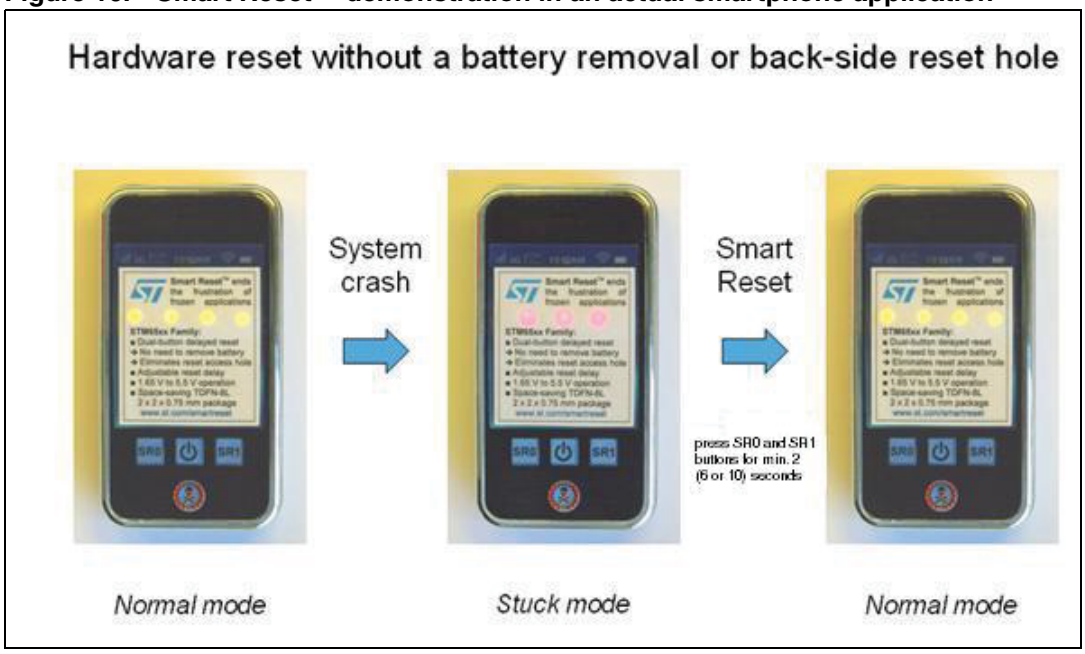
The STM65xx smartphone demonstration shows the Smart Reset™ concept and functionality in a real application (dual push-button delayed reset):

Figure 9. Smartphone demonstration example shows STM6503 implemented in an actual application

Smart Reset™ concept demonstration

- Push ON/OFF button → goes into a normal ON state (amber display backlight on)
- Push stuck button → goes into stuck mode that simulates frozen smartphone (red display backlight on) during which it cannot even be turned off
- Push SR0 and SR1 buttons simultaneously for 2 (6 or 10) seconds minimum (jumper-selectable) → returns to the normal state from which it can be turned off by pressing the ON/OFF button

Figure 10. Smart Reset™ demonstration in an actual smartphone application


Hardware reset without a battery removal or back-side reset hole
System crash
Smart Reset
press SR0 and SR1 buttons for min. 2 (6 or 10) seconds
Normal mode
Stuck mode
Normal mode

4 Conclusion

The family of Smart Reset™ devices provides a variety of smartphone or PDA hardware reset solutions, some examples of which are shown in this application note, others are in the datasheet of the specific device. The most up-to-date information on the Smart Reset™ portfolio can be found at *www.st.com/smartreset*.

5 Revision history

Table 1. Document revision history

Date	Revision	Changes
22-Sep-2010	1	Initial release.

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